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UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN JOSE DIVISION

VERIGY US, INC., a Delaware Corporation) Civil Case No.: C07-04330 RMW (HRL)

Plaintiff:

VS.

ROMI OMAR MAYDER, an individual,
WESLEY MAYDER, an individual,
SILICON TEST SYSTEMS, INC. a
California Corporation, SILICON TEST
SOLUTIONS, LLC, a California Limited
Liability Corporation, inclusive,

Defendants.

Civil Case No.: C07-04330 RMW (HRL)

**DECLARATION OF FRANK
SWIATOWIEC, FORMERLY CEO
OF NANONEXUS**

Date: N/A
Time: N/A
Dept.: Judge: Hon. Judge Whyte

1 I, Frank Swiatowiec, declare as follows:

- 2 1) I have personal knowledge of all the facts set forth in this declaration and, if called upon to
3 testify in this Court as to those facts, my testimony would be as stated herein.
- 4 2) I am now CEO of a new company, but for nearly five (5) years I was founder and Chief
5 Executive Officer ("CEO") of NanoNexus. NanoNexus, then and now, manufactures
6 advanced contactor and interconnect products for the electronics industry. Specifically for the
7 semiconductor test industry NanoNexus manufactures probe cards that interface between
8 memory testers, such as those manufactured by Teradyne or Advantest, and the device under
9 test ("DUT") (in this application a semiconductor wafer). Exhibit A contains a true and correct
10 copy of exemplary picture of a NanoNexus probe card.
- 11 3) The NanoNexus probe card (and most other probe cards) performs two major functions; (1)
12 enables memory testers to electrically contact the pads of the wafer under test, and (2) it
13 shares resources of the tester by utilizing its resources more effectively.
- 14 a) In general, all probe cards interconnect the memory tester connections (channels) with a
15 wafer. The process of making this connection is known as a "touchdown" and requires
16 extreme accuracy in placement of the probe card on the wafer and precision in electrically
17 contacting the pads on the wafer. The greater the density of probes that can be precisely
18 and accurately manufactured, the greater the number of DUTS that can be tested in
19 parallel.
- 20 b) By including (or attaching) electronics on the probe card, significantly more DUTS can be
21 tested without increasing the number of tester channels.
- 22 i) For example, I am aware of probe cards that "fan out" one memory tester channel to
23 two or more pads on the wafer. This essentially allows the memory tester to test two
24 wafer pads with one channel.

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- 1 ii) Also, by including semiconductor switches on the probe card, a memory tester channel
2 can be *selectively* routed to a pad on the wafer.
- 3 iii) Depending on the speed needed, there exists many semiconductor switches available
4 off the shelf from semiconductor manufacturers that can be used to implement this
5 selective routing capability on the probe card.
- 6 4) While CEO of NanoNexus we designed and manufactured many such "resource sharing"
7 probe cards for our customers. The use of "fan-out" with probe cards for testing of memory
8 devices were already in existence when we started entering the memory market in the year
9 2001.
- 10 5) While at NanoNexus we did not consider our use of these resource sharing technologies trade
11 secret because they were well known and used in the industry by probe card manufacturers
12 (such as ourselves), memory manufacturers (our customers), and tester manufacturers (such as
13 Teradyne – a Verigy competitor). Specifically, while at NanoNexus we manufactured probe
14 cards compatible with Advantest and Teradyne systems.
- 15 6) I have read papers discussing resource sharing solutions of the type discussed above that have
16 been publicly presented at semiconductor test conferences. Attached as Exhibit B is a copy of
17 the pertinent portions of such a presentation from the 2007 Semiconductor Wafer Test
18 Workshop.

21 I declare, under penalty of perjury the foregoing is true and correct, executed this 27th day of
22 September 2007 in San Jose, California.

24 Frank Swiatowiec
25 Frank Swiatowiec